

SPSC

substrate 20 abuts or is positioned in close proximity to the facing surface 24, 14 of the other of test substrate 20 or semiconductor device 10, respectively. As is known in the art, compressive forces may be applied to semiconductor device 10 or test substrate 20 during assembly, while semiconductor device 10 is being tested, or during disassembly.

5 Accordingly, contact surface 52 and the portion of each stabilizer 50 contacting surface 14 or 24 are preferably sized and configured to spread or distribute any compressive forces that may be applied to semiconductor device 10 or to test substrate 20 over relatively large areas of semiconductor device 10 and test substrate 20. By spreading such compressive forces over larger areas of semiconductor device 10 or test
10 substrate 20, damage to semiconductor device 10 or to test substrate 20 that could otherwise be caused by such compressive forces can be prevented. Stabilizers 50 can also be arranged or positioned so as to minimize the likelihood that compressive forces on semiconductor device 10 or test substrate 20 will damage either semiconductor device 10 or test substrate 20.

15 In addition, stabilizers 50 are configured to have sufficient strength and rigidity to withstand the assembly of semiconductor device 10 with test substrate 20, the testing of semiconductor device 10 on test substrate 20, and the disassembly of semiconductor device 10 from test substrate 20. When disposed on test substrate 20, stabilizers 50 should withstand repeated series of assembling, testing, and disassembling. When
20 disposed on semiconductor device 10, stabilizers 50 are preferably configured to substantially maintain their configurations, dimensions, strength, and rigidity during any subsequent processing of semiconductor device 10, as well as during normal operation of semiconductor device 10.

25 In addition, stabilizers 50 are preferably configured to, along with conductive structures (e.g., solder bumps 30) protruding from semiconductor device 10, prevent tipping or tilting of semiconductor device 10 relative to test substrate 20.

Although stabilizers 50 are depicted in FIGs. 5 and 7(H) as each having a cylindrical shape, stabilizers 50 may alternatively be configured as pillars having a rectangular cross-section (FIG. 7(A)), pillars of triangular cross-section (FIG. 7(B)),